## Amendments to the Specification

Please replace the paragraph at page 3, lines 17-25, with the following amended paragraph:

According to this principle, a byte-interleaving multiplexer intermittently transmits bytes of the 10 containers via an optic link in a manner that specific time slots are assigned to bytes of the respective specific containers. Let the optic link allows allow for transmitting bytes in 16 timeslots, with a frequency 2.5 GHz, which is sufficient for a high rate SDH signal STM16. For example, the initial arrangement at the transmitter side is such that bytes of VC4 containers Nos.1 to 5 are sent in respective time slots 1 to 5, and bytes of VC4 Nos.6 to 10 are transmitted in time slots 9 to 13.

Please replace the paragraph at page 16, line 24 to page 18, line 17, with the following amended paragraph:

Fig. 1 illustrates a schematic block-diagram of the basic embodiment 10 of the proposed system for rearrangement of data streams. The system comprises a 1<sup>st</sup> node 12 connected to the 2<sup>nd</sup> node 14 by a telecommunication path 16 in a network 17, in this embodiment the path constitutes a single transmission link. It should be noted that two or more parallel links may be provided to interconnect the nodes 12 and 14. The system also comprises a network manager block 15 connected to control units 11 and 13 of the first and second nodes, respectively. An incoming original data stream, generally marked 18, arrives to the system in the demultiplexed form. For example, the

original data stream carries eight fragment data streams (fragments) VC4 occupying all odd time-slots (schematically indicated as S1, S3, S5...S15) from the available sixteen time slots of the original data stream. All even slots of the data stream are vacant (S2,...,S16). Suppose that required to transmit a new signal VC4-4c (a concatenated data stream) using the timeslots which remain available in the original data stream. (Examples of the particular data streams in the drawings are not limiting). We remember that the mentioned new signal called VC4-4c needs four consequent timeslots for its transmission. Though there are eight vacant time-slots in the data stream 18, the requirement cannot be met at the present arrangement, since the vacant time-slots are "loosely spread" over the data stream. To resolve the problem, the following exemplary system is proposed by the invention. All the basic fragments are applied to the input stage of a cross-connect 20 of the first node 12 (i.e., the  $1^{\rm st}$ In this example, the cross-connect 20, under cross-connect). control of the network manager 15 via the control unit 11, copies (doubles, or "bridges") two fragments following in the time-slots S1 and S3 so that at the output stage of the crossconnect 20 two identical fragments can be found for each basic fragment. In particular, the 1st cross-connect 20 performs connections so that the basic fragment VC4A appears at the output stage at a contact assigned to the time slot S1, and a copy fragment VC4a appears at a contact of the output stage, associated with the time-slot S6. In this particular example, the number of the basic fragments which has been copied is 2 i.e., n=2. Α TDM multiplexer 22 provides equal to multiplexing of all the fragments outgoing from the output stage of the cross-connect 20, according to their assigned time slots and transmits via the communication link 16 an

intermediate data stream marked  $18+\Delta$ . The intermediate data stream comprises all the fragments of the original data stream 18 and additional two copied fragments (VC4a and VC4b). TDM demultiplexer 24 the second node 14, a splits the into the component fragments, intermediate data stream whereupon the delay equalization is provided in block 26. In this example, the delay equalization is effected for the two copied pairs of fragments: VC4A relative to VC4a, and VC4B relative to VC4b. The delay equalizing block 26 is controlled by the control unit 13 and is capable of applying its functions to any pair of fragments indicated by the control unit. The fragments, which underwent the delay equalization, are marked with (') in Fig. 1. The control unit 13 ensures that the 2<sup>nd</sup> cross-connect 28 takes care of all fragments except for the fragments VC4A' and VC4B' (i.e., no output contacts are created for these two fragments at the output stage of the cross-connect 28).

Please replace the paragraph at page 18, line 24 to page 19, line 13, with the following amended paragraph:

Fig. 2 shows the block-diagram of Fig. 1 with changes which can be introduced upon forming the rearranged data stream 18R. The control unit 13 of the first second node communicates with the network manager 15, and the latter instructs the control unit 11 of the first node. The 1st crossconnect 20, according to a command provided by the control unit 11, drops internal connections between the incoming "n" original data fragments and the outputs assigned to their original time-slots. Consequently, the intermediate

data stream becomes equal to the rearranged data stream and, beginning from the output stage of the 1<sup>st</sup> cross-connect 20 up to the output stage of the 2<sup>nd</sup> crossconnect 28, the first four time-slots S1 to S4 become vacant. The rearrangement is completed. One of the results is that the network is optimized. Actually, optimization of the network may be the sole object of the rearrangement operation. One example of rearrangement provided in order to optimize transmission of the initial data stream in the network between two reference nodes will be illustrated in Fig. 4. The system shown in Fig. 2 is now ready for transmitting a new signal in addition to the rearranged data stream. The following stage is illustrated in Fig. 3.

Please replace the paragraph at page 23, line 11 to page 24, line 21, with the following amended paragraph:

For example, a fragment comprising VC4A (which initially occupied one of the original time-slots) enters branch 32 of the unit 30 and its payload is ready to be fed to a FIFO memory block 38. A Pointer Interpreter (block 36) watches pointers of a particular frame of the fragment VC4A and transmits the information to a Pointer Generator block 40. the initial shift of the pointers According to increment/decrement), the informational payload of the frame will be written into the FIFO 38 (see the commands "enable" and "write"). Information on the initial increment/decrement of the pointers is entered into the Pointer Generator Block 40. Information on the state of FIFO 38 is also introduced into the block 40. Based on the pointers' initial position, the FIFO clock and the outgoing signal clock, the Pointer Generator 40 prepares pointers of the outgoing signal (actual pointers). Similar operations are performed at the branch 34 with the copy fragment VC4a (which is intended to occupy a vacant time slot). Each of the Pointer Generators 40 and 41 informs the control unit 13 about the corresponding actual 35). pointers' position (arrows 33 and Based on this information, the control unit 13 issues to at least one of the Pointer Generators an increment/decrement request (arrows 47 43 and/or 45), so as to synchronize the timing of the two payloads under treatment by influencing pointers suitable fragment's frame. According to one embodiment of the delay equalizing means, the increment/decrement requests are introduced with the aid of software of the network manager. requests <del>47</del> 43, 45, issuance of the the generators 40 and 41 issue suitable increment/decrement instructions (which retard or accelerate the frame) to the respective FIFO blocks 38 and 39, thereby changing depths of the FIFOs. The two payloads, while being read from the FIFO blocks, are accompanied by newly generated pointers, which incorporate the requested increment(s)/decrement(s). The two frames can then be issued from the parallel branches of the unit, as portions of synchronous fragments VC4A' and VC4a'; timing of the payloads in these frames will be identical. However, only one of the fragments (namely, the copy VC4a') will be enabled by the control unit 13 to enter the 2<sup>nd</sup> crossconnect 28. As a result, the 2<sup>nd</sup> cross-connect will create internal connection only for this fragment, out of the two illustrated in Fig. 4, so as to output the copy fragment VC4a' in the combination of the rearranged data stream (not shown). Actually, the enabling instruction of the block 13 may be used to output from the delay equalizing unit 30 only the selected fragment while blocking the second one.